

Voltage Boosted Fail Detecting Circuit for Selective Write Assist and Cell Current Boosting for High-Density Low-Power SRAM

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Abstract—In low supply voltage (V_{DD}), the wordline (WL) underdrive read assist and the negative bitline (NBL) write assist circuits are widely used for stable operation of SRAM. However, NBL consumes enormous energy and WL underdrive read assist degrades performance. A voltage-boosted fail-detecting circuit for selective write assist (VBFD-SWA) and selective cell current boosting (VBFD-SCCB) is proposed for high-density low-power FinFET static RAM (SRAM). VBFD-SWA detects the bitline status and then selectively triggers NBL only when a write failure is detected, reducing the write energy consumption. VBFD-SCCB detects slow bitcell and selectively triggers cell current boosting to improve read performance. The simulation results show that the write energy consumption is improved by 19% and the read performance is improved by 36% by applying the VBFD-SWA and VBFD-SCCB, respectively, with an area overhead of 10%.

Index Terms—Low-power static RAM (SRAM), SRAM write-assist circuit, SRAM read-assist circuit.

I. INTRODUCTION

AS THE demand for wearable devices and the Internet of things (IoT) grows, the importance of low-power and high-performance system-on-chip (SoC) is increasing. Static random-access memory (SRAM) is one of the main components of a SoC. One simple way to achieve low-power SRAM is lowering the supply voltage (V_{DD}); however, lowering V_{DD} degrades stability and performance. Recently, it has become common to use assist circuits for read and write operations to maintain the stability and performance of SRAM in low V_{DD} . The assist circuits dynamically adjust the bitcell control signals to make the bitcell robust to operation failures.

The read-assist circuits are divided into column-based assist circuits and row-based assist circuits. The row-based circuit is the wordline (WL) underdrive circuit. The column-based assist circuits, such as boosting cell V_{DD} (CVDD) or cell V_{SS} (CVSS) [1], cause a large dynamic power overhead.

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On the other hand, the row-based WL underdrive read assist circuit (WLUD-RA) causes relatively less power overhead as well as relieves row half-selected cells (RHSCs) issues. For those reasons, WLUD-RA is most frequently used [2], [3], [4]. However, WLUD-RA degrades the write ability and read performance because reduced WL weakens pass-gate (PG) transistor strength, especially in low V_{DD} .

WL overdrive (WLOD) [5], [6], transient voltage collapse (TVC) [7], [8], [9], raising CVSS [10], [11], and negative bit-line (NBL) [12], [13], [14], [15] are used for write assist techniques. Although TVC and NBL effectively increase the write ability without harming the half-selected bitcells, they inevitably incur large power consumption. This is because TVC results in massive pull-down current to change CVDD node with a large capacitance, and NBL normally uses a huge coupling capacitor to change bitline (BL) with a large capacitance.

To reduce the write assist power, selective negative bitline write assist (SNBL-WA) [12] technique is proposed. However, write failure detecting takes too much time because a static CMOS inverter is used for the write failure detector. In order to avoid this problem, a complex BL precharge conditioning circuit is used. However, the additional BL conditioning makes the circuit more complex and susceptible to noise. In [16], the conditional biasing WA (CBWA) is proposed, which utilizes floating CVSS for the write assist to decrease power overhead. However, it takes a significant amount of time to raise CVSS, because large CVSS capacitance should be charged with weak bitcell transistors. Thus, it is highly challenging to achieve the target write yield without speed degradation.

Write- and performance-assist cell (W- and P-AC) circuit [17] is proposed, which restores BL and WL during write and read operation, respectively. These circuits increase the write ability by reducing the effects of interconnect parasitic resistance. However, compared to the write assist circuits that directly boost BL or collapse supply voltage, the write ability enhancement effect is highly limited. In [18], [19], and [20], the charge recycling or redistribution techniques are used to reduce the power overhead of the write assist. However, in [18] and [19], the CVSS boosting during write operation inevitably degrades the half-selected bitcell stability, while in [20], the requirement for an additional phase to charge sharing significantly increases the cycle time.

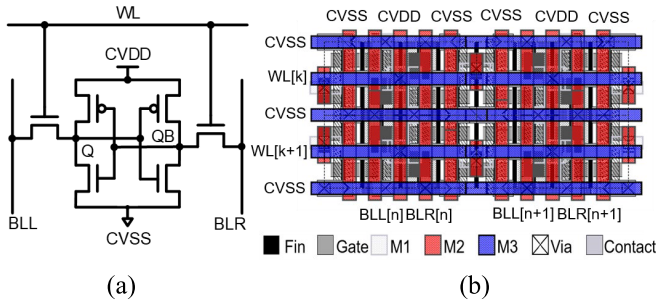


Fig. 1. Structure of the conventional 6T SRAM bitcell: (a) schematic and (b) layout by 2×1 bitcell.

In this study, we propose read and write assist circuits with BL status sensing to address the read performance degradation and large write assist energy overhead. First, unlike the conventional NBL, our proposed selective write assist circuits do not generate the NBL for every write operation. Instead, the write assist is generated only when the write failure is detected by the BL status sensing. Thus, the write assist power can be saved without performance degradation. Second, the BL status sensing circuit is also used to detect slow bitcell and trigger cell current (I_{CELL}) boosting to improve the read performance. Again, the I_{CELL} boosting is enabled only for the slow bitcells, so the power overhead is minimized. It should be noted that the same BL status sensing circuit is used to save the write energy, improve read performance, and reduce the circuit overhead.

In the next section of this paper, the background is explained. Then, Section III describes the structure and operation of the proposed selective write assist circuits through BL status sensing. In Section IV, selective I_{CELL} boosting is presented using the same sensing circuit. Section V describes the simulation results and compares the proposed structure with that of the conventional SRAM. Finally, Section VI concludes the study.

II. BACKGROUND

A. SRAM Bitcell Structure

Fig. 1(a) and (b) show the schematic and layout of the conventional 6T SRAM bitcell, respectively. The layout is shown in Fig. 1 (b), based on 7nm ASAP technology [21]. Bit-line pairs (BLL and BLR) and CVDD are routed vertically with M2, while CVSS is routed using M2 and M3 for power mesh, and WLs are routed horizontally with M3.

B. SRAM Read Operation and Assist Circuits

The read operation of SRAM is performed by sensing the voltage difference between BL pairs, which are pre-charged to V_{DD} . When the WL is asserted, one of the BLs is discharged to a low voltage level according to the stored data in the bitcell. After BL discharges enough to meet the read sensing yield, sense amplifier enable signal (SAE) is engaged. Then, from the voltage difference of BL pairs, SA reads the data whether “low” or “high.”

Fig. 2 shows the state of the bitcell and the waveform for the read operation. It is assumed that the initial condition of the

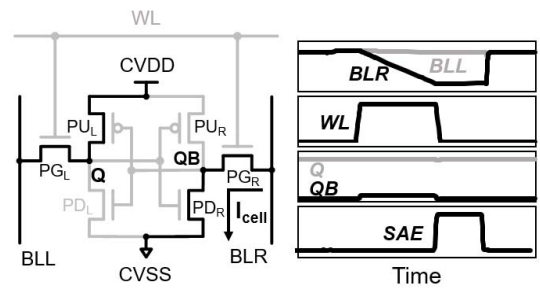


Fig. 2. Conventional 6T SRAM bitcell read operation and waveforms.

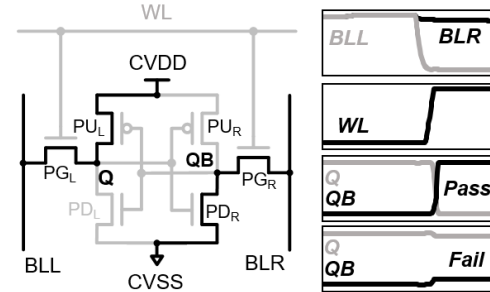


Fig. 3. Conventional 6T SRAM bitcell write operation and waveforms corresponding to write pass and fail.

left bitcell storage node (Q) is “high” and that the right node (QB) is “low”. When the BLR is discharged, the voltage of QB increases due to I_{CELL} through the PG_R . If QB is over the voltage trip point of the inverter, the stored data in the bitcell is flipped, which results in read failure. To alleviate this read failure, the driving strength of the PG must be weaker than that of the pull-down (PD). As previously stated, the WLUD-RA technique is frequently used to improve read stability by suppressing the WL voltage level. However, underdrive WL decreases I_{CELL} , which results in serious read performance degradation, especially in low V_{DD} .

C. SRAM Write Operation and Assist Circuits

Fig. 3 shows the SRAM bitcell under the write operation and the waveform for the write pass and fail. Assuming that $D = 0$ is written when the selected bitcell initially stores $Q = 1$ and $QB = 0$, BLL is discharged to GND. There is a conflict between PU_L and PG_L after WL is enabled at the Q node. For the successful write operation, the drive strength of PG_L should be sufficiently larger than that of PU_L .

When using WLUD-RA, which is common in low V_{DD} , WL should be underdriven for read operations as well to protect the row half selected bitcells from data flip. Accordingly, WLUD-RA weakens PG, resulting in decreased write stability. As a result, the write assist circuit is required to meet the target write yield. The negative BL write assist circuit (NBL-WA) is one of the most widely used techniques, which biases low BL to a negative voltage instead of GND. Fig. 4 shows the conventional NBL-WA structure and waveforms. After the negative enable signal (/NegEn) is enabled, NVSS which supplies the write driver falls to a negative voltage through

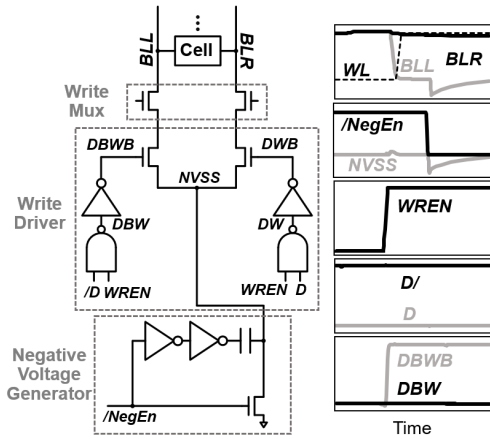


Fig. 4. Conventional NBL-WA structure and waveforms.

capacitive coupling. In order to discharge BL to a negative voltage, the coupling capacitor should be large because of the high BL capacitance. Thus, NBL-WA which is triggered for all the selected columns for every write operation incurs a significant amount of dynamic energy overhead.

III. SELECTIVE WRITE ASSIST CIRCUIT

As explained, the use of the conventional NBL-WA results in a huge dynamic power overhead. In particular, assisting every bitcell for every write operation is an inefficient way in terms of energy, because write can be successfully performed without assist circuits for most bitcells. To resolve this issue selective write assist, which is enabled only when the write assist is required, is proposed in this section.

The structure of the proposed voltage boosted fail detecting selective write assist (Vbfd-SWA) circuit is shown in Fig. 5. It should be noted that a voltage boosted failure detecting (Vbfd) circuit is implemented to selectively assert /NegEn by sensing BL states. In Vbfd, M_{PDL} and M_{PDR} are used to sense the voltages of BLL and BLR, respectively. The supply voltage of M_{PDL} and M_{PDR} , V_{DDH} , is designed to be raised through coupling capacitor C_{C0} , while C_S is used for the storing capacitor. For reasons to be explained later, M_{P2} is added to form the positive feedback between /NegEn falling and OUT rising. The overall operation of Vbfd-SWA is composed of three steps: 1) The BLs are first driven by write drivers without NBL-WA, 2) whether write failures or successes for the selected bitcell are detected, and 3) NBL is enabled only when write failures are detected, but not enabled when write successes are detected.

Fig. 5(b) shows the write operations of Vbfd-SWA. It is assumed that $D = 0$ is written, while the selected bitcell initially stores $Q = 1$. At the beginning of the write operation, M_{N0} is turned on by high /SEL. Thus, $OUT = 0$ and /NegEn = 1, which drives NVSS to GND. DBWB becomes high after WREN is asserted by being pulled up, while DWB stays low ($\because D = 0$). Thus, the selected BLL where write MUX is on is driven to GND by M_{N1} , while BLR is floated. At the same time, in Vbfd, overdrive enable signal (ODEN) is raised to turn off M_H and boost

V_{DDH} to $V_{DD} + |V_{th,MPD}|$. Then after SEL is raised, M_{PCHL} , M_{PCHR} , and M_{N0} are turned off, while M_{PL} and M_{PR} are turned on. It should be noted that in the proposed Vbfd, the conventional read MUX control signal is replaced with a combination of column select signal (ColSel) and DW or DBW. In order to make one of the read MUX is turned on during the write operation according to the write data value. Thus, M_{RMXR} is turned on to connect BLR to X_R .

The operational waveforms are shown in Fig. 5(b) for two cases: 1) write success without NBL-WA and 2) write initially fail without NBL-WA, so the NBL-WA is required to trigger for write success. If write succeeds without NBL-WA trigger, BLR stays near V_{DD} so $|V_{GS}|$ of M_{PDR} is almost the same as $|V_{th}|$. Thus, current barely flows through M_{PDR} , so OUT is kept low until the end of the write operation. On the other hand, if write fails without NBL-WA storage data Q and QB are not flipped, Q is high, and QB is still low. Owing to low QB, floated ‘‘high’’ BLR is slowly discharged like the read operation. As a result, after the SEL is enabled the lower BLR causes $|V_{GS}|$ to exceed $|V_{th}|$ in M_{PDR} , resulting in current flow from V_{DDH} to OUT. This makes OUT be pulled up, then /NegEn is pulled down which triggers NBL-WA. To fully charge OUT to V_{DD} even with a small current through M_{PDR} , the positive feedback circuit of M_{P2} , which is triggered by lowered OUTb, is added.

Fig. 6 shows the flow chart and its matched waveforms for control signals of Vbfd-SWA to understand the operation more clearly.

V_{DDH} is designed to be overdriven to the $V_{DD} + |V_{th,MPD}|$. This is because if V_{DDH} exceeds $V_{DD} + |V_{th,MPD}|$, M_{PDS} (M_{PDR} and M_{PDL}) are turned on. Then V_{DDH} is discharged through M_{PDS} until V_{DDH} becomes $V_{DD} + |V_{th,MPD}|$, and M_{PDS} are turned off. It should be noted that this process does not affect node OUT, because SEL is not enabled yet, and OUT stays low by turning on M_{N0} . Accordingly, boosted level of V_{DDH} can track the V_{th} variation of M_{PDS} , where $|V_{th,MPD}|$ is the smaller one between $|V_{th,MPDL}|$ and $|V_{th,MPDR}|$. Thus, the current through M_{PD} is robust on the V_{th} process variation, leading to preventing unexpected leakage current which flows through M_{PDS} and M_H . To realize this, V_{th} tracking M_{PDS} are designed with LVT, while M_H is designed with RVT.

Capacitor C_{C1} in negative voltage generator (NVG) is set to satisfy the target write yield ($= 6\sigma$), and C_{C0} is used to be large enough to boost V_{DDH} to $V_{DD} + |V_{th,MPD}|$. To achieve the target write yield when Vbfd-SWA is used, /NegEn should be properly lowered whenever the write failure occurs. Accordingly, C_S should be set large enough for V_{DDH} node stores enough charge to fully pull OUT up when M_{PD} is turned on by write failure. In addition, the time duration of the SEL (T_{SEL}) should be set large enough to provide sufficient time for OUT to be reached to V_{DD} by M_{PD} current. On other hand, too large C_S or long T_{SEL} raises OUT even for write success case. This means that an unnecessary write assist is performed, wasting energy consumption. In this context, the write assist rate should be minimized to reduce energy overhead, provided that the target write yield is satisfied. Thus, C_{C0} , C_S , and T_{SEL} should be carefully optimized.

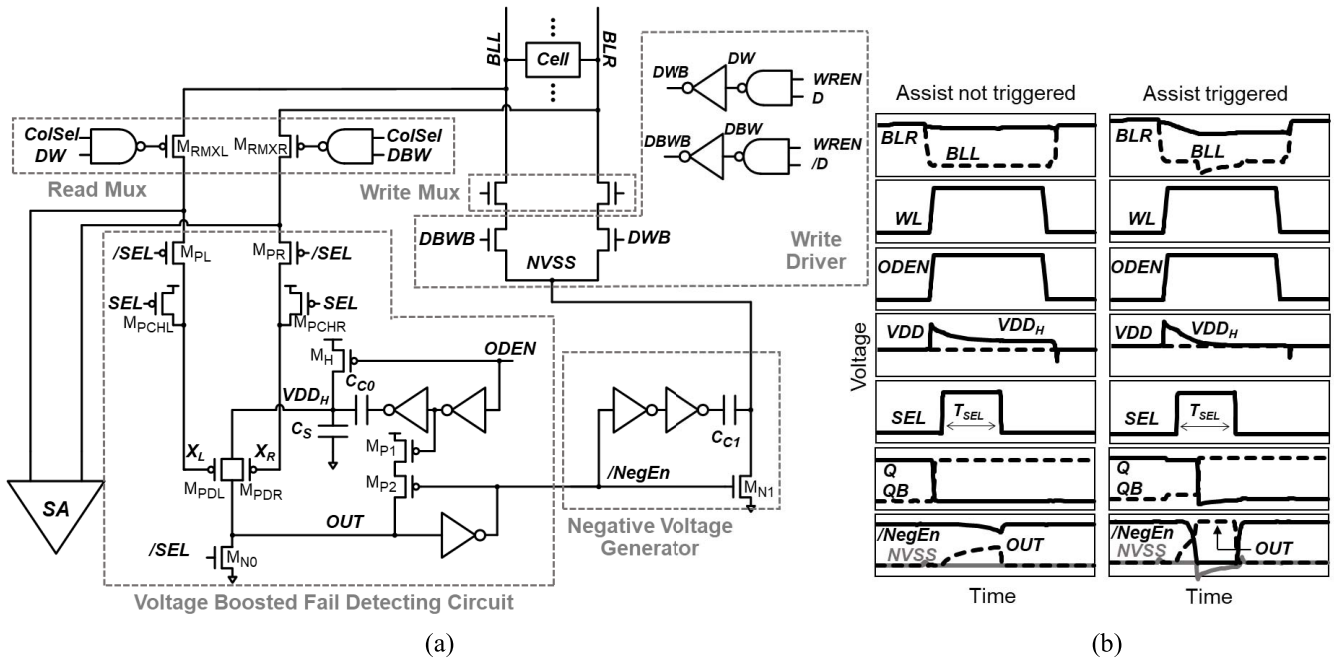


Fig. 5. Proposed VBFD-SWA structure (a) and operational waveforms (b) when write assist not triggered and assist triggered.

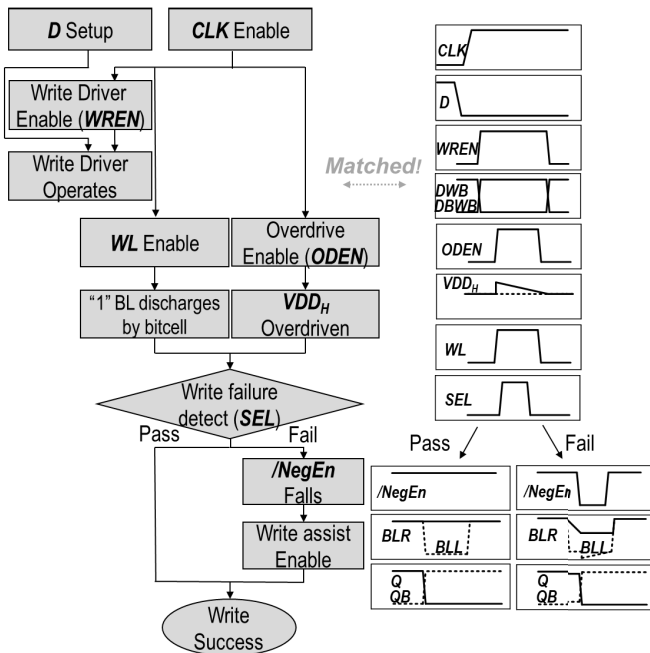


Fig. 6. Control signal flow chart of VBFD-SWA and its matched waveforms.

Fig. 7 shows the write yield and assist rate according to three different parameters of C_S and T_{SEL} at the fixed C_{CO} of 1.5 fF. The results are derived from an HSPICE Monte Carlo (MC) simulation with the most probable failure point (MPFP) [22], V_{DD} is 0.6 V and WL underdriven voltage (V_{WL}) is 0.52 V. The global process corner is TT and the temperature is set to -40°C (the worst temperature for the write ability). To achieve the target write yield of 6σ as mentioned before, C_S should be large. Large C_S (1.8 fF) not only results in a

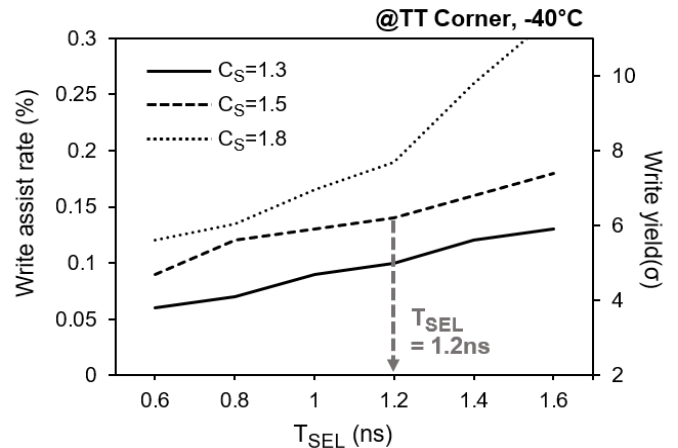


Fig. 7. Write yield and write assist rate according to T_{SEL} and C_S .

high write yield but also generates an excessive write assist ratio. In the same context, T_{SEL} becomes larger, assist rate and write yield are increased rapidly. To minimize the assist rate, while meeting the target write yield, $T_{SEL} = 1.2\text{ ns}$, and $C_S = 1.5\text{ fF}$ are chosen, and that of write assist ratio is 14% which is obtained from MC simulation.

For the two capacitors (C_{CO} , C_S) optimization, Fig. 8 shows the shmoo plot of the write operation for different values of C_S and C_{CO} for the target write yield of 6σ at the fixed T_{SEL} of 1.2 ns. Among the options satisfying target write yield, $C_{CO} = C_S = 1.5\text{ fF}$ are chosen to minimize area overhead and maximize power saving. In addition, by choosing these balanced capacitor sizes for C_{CO} and C_S , the capacitance variation can be minimized by avoiding using small capacitance [23].

In addition, even if the slow bitcell is accessed, OUT should be raised as quickly as possible to make the whole

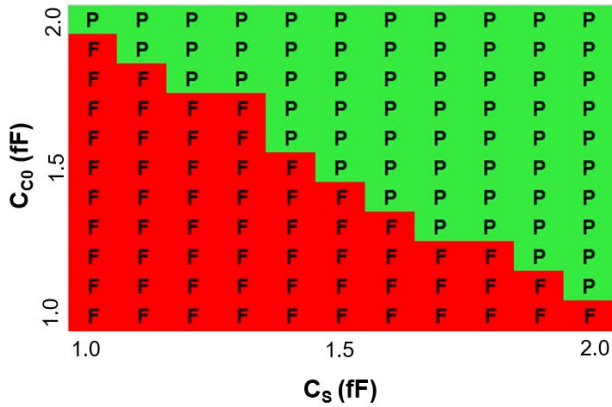


Fig. 8. Shmoo plot of write operation that satisfies target write yield of 6σ for different values of C_s and C_{C0} .

VBFD-SWA operation complete within the WL duration pre-determined by the read operation. To achieve this goal, the capacitance of OUT is reduced by minimizing the size of M_{PDL} , M_{PDR} , M_{N0} , M_{P2} , and CMOS inverter driven by OUT. Then, C_{C0} and C_s are adjusted properly. Thus, VBFD-SWA is carried out within WL duration with the minimized transistors used for the components that are connected to OUT and with adjusted C_{C0} and C_s , without the cycle time overhead.

IV. SELECTIVE CELL CURRENT BOOSTING CIRCUIT

As previously mentioned, the use of WLUD-RA in low V_{DD} significantly degrades the read performance. To resolve this problem, the I_{CELL} can be boosted by driving CVSS to a negative value at the expense of energy increase. To minimize the energy overhead, the I_{CELL} boosting can be applied only for the slow bitcells, which critically determine the overall read speed. In this section, we propose a VBFD-based selective cell current boosting circuit (VBFD-SCCB), which reuses VBFD proposed in Section III. By sharing VBFD with the NBL-WA, the proposed scheme can be implemented in an area-efficient way. Besides the speed, energy can be saved through the proposed VBFD-SCCB. In the read, and write operation most BLs are unnecessarily discharged into both the selected and unselected columns, occupying a large portion of total energy consumption. The reduced WL duration (RWL) by the proposed VBFD-SCCB can decrease the BL discharge amount, leading to energy savings.

Fig. 9(a) and (b) show the schematic and operational waveforms of the proposed VBFD-SCCB, respectively. It should be noted that VBFD is shared with VBFD-SWA, which is used for sensing BL status. We shared the same capacitance of C_{C1} , which is used as a negative voltage generator in both the VBFD-SWA and VBFD-SCCB for area efficiency. Utilizing VBFD, the slow bitcell can be detected to selectively trigger I_{CELL} boosting. To incorporate the I_{CELL} boosting operation, two transmission gates – TG_1 and TG_2 – and a NAND2 gate are added. TG_1 and TG_2 are both designed to turn on when SRAM read and write operations are not enabled, while during the operation, one of the TGs is turned off depending on the READ and WREN signals. For read operation, by $READ = 1$,

TG_1 is turned off, and TG_2 is still turned on. NAND2 is triggered by the read select signal (RSEL), which is enabled only when performing a read operation.

To keep switching CVSS connection nodes, which are GND or negative voltage, CVSS footers – M_{FT1} and M_{FT2} – are added. Through the M_{FT1} and M_{FT2} , depending on BLRS, CVSS is connected to the NVSS or GND. In addition, CVSS is separately routed column-by-column, as shown in Fig. 10. It should be noted that compared with the conventional structure shown in Fig. 1(b), the effective resistor from GND to CVSS is increased, and the capacitance of CVSS is decreased.

Fig. 9(b) shows the read operation for the two cases which are nominal and slow bitcell, where the SCCB is triggered only for the slow bitcell. For the read operation, it is assumed that the bitcell storage data $Q = 1$, after WL enable BLR is discharged and OUT is low before $/SEL$ enables. Then, ODEN is raised to turn off M_H and boost V_{DDH} to $V_{DD} + |V_{thp,MPD}|$. Until now, the operation of VBFD has been the same as in Section III. Then from DW and DBW which are both high ($\therefore WREN = 0$), both M_{RMXR} and M_{RMXL} are also turned on.

In a slow bitcell, OUT is still low because BLR is not enough to fall to turn on M_{PDR} , which means $OUTb$ is also still high. Consequently, after RSEL is enabled, NAND2 is triggered and $/NegEn$ is generated to generate negative NVSS, resulting in a CVSS pull down to a negative voltage and boosting the I_{CELL} . When RSEL is enabled in a nominal bitcell, OUT is generated to high and $OUTb$ is pulled down to low. Thus $/NegEn$ stays high and CVSS is kept connected to GND, which means I_{CELL} boosting is not asserted. To understand the operation more clearly, the flow chart and its matched waveforms for control signals of VBFD-SCCB are shown in Fig. 11.

In the VBFD circuit, BL failure detection is achieved both in read and write operations, thus NAND2 gate and RSEL are applied to trigger NVG to distinguish read and write detection. It should be noted that the timing of RSEL is carefully determined. First, the rising time of RSEL should be waited for to provide enough time for $OUTb$ to pull down for the nominal bitcell case. In this manner, unnecessary I_{CELL} boosting is prevented to minimize the energy overhead. Second, the time duration of RSEL (T_{RSEL}) should be considered. T_{RSEL} is equal to the time duration of overdriving CVSS. If T_{RSEL} is not large enough, the slow BL is not discharged to the target level enough for SA to sense data stably. On the contrary, if T_{RSEL} is too large, unwanted read assist frequently occurs, increasing the energy overhead. Fig. 9(b) in the slow bitcell shows an example of the role of RSEL, although $OUTb$ is triggered to “high” at the end of T_{SEL} , RSEL is already turned off, then assist does not occur. Thus, T_{RSEL} should be large enough to sufficiently improve the sensing yield, while minimizing the unwanted read assist for energy saving.

Fig. 12 shows the time duration of WL (T_{WL}) improvement and read energy according to T_{RSEL} . The simulation result of T_{WL} is derived from an importance sampling [24], [25]; V_{DD} is 0.6 V and V_{WL} is 0.52 V, whereas V_{WL} is under-driven and determined to obtain target read stability yield. When T_{RSEL} becomes large, T_{WL} becomes short, and the energy is de-creased thanks to reduced WL (RWL). However,

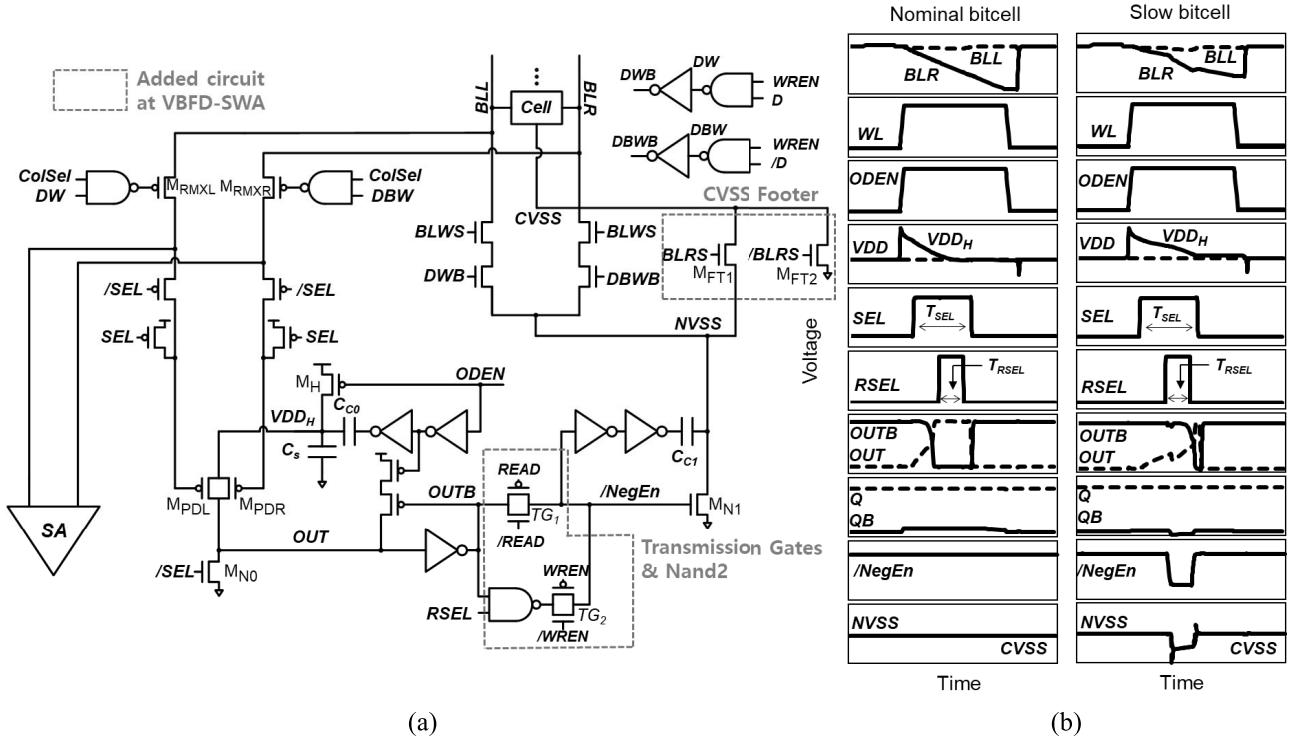


Fig. 9. Proposed VBFD-SCCB structure (a) and operational waveform (b) when nominal bitcell not triggered cell current boosting and slow bitcell triggered cell current boosting.

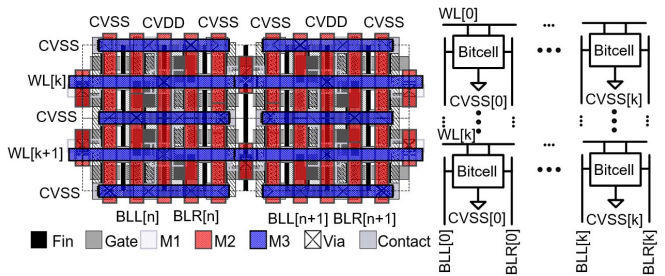


Fig. 10. Layout of separated CVSS column routing and the associated SRAM array.

if T_{RSEL} is over 0.7 ns, T_{WL} is not decreased anymore. Thus, we determine T_{RSEL} is 0.7 ns, that of T_{WL} improvement is 36% (2.6 ns \rightarrow 1.67 ns), and that of read energy is 27.7 fJ.

V. COMPARISON

All simulation results are based on 7-nm ASAP FinFET post-layout simulations. We compare the proposed VBFD-SWA and VBFD-SCCB with the conventional SRAM design in terms of power, performance, and area (PPA). The SRAM bitcell array size of 256 rows, 128 columns, and 4-to-1 BL MUXs is considered and a conventional voltage latched sense amplifier (VLSA) is used. V_{DD} is 0.6 V and 5% worst voltage corner is considered, and V_{WL} is 0.52 V, which is determined to require a target read stability yield of 6σ .

To evaluate each SRAM design, MC and HSPICE simulations were performed with V_{th} variation. To model the transistor's variation, V_{th} is assumed to follow Gaussian distribution

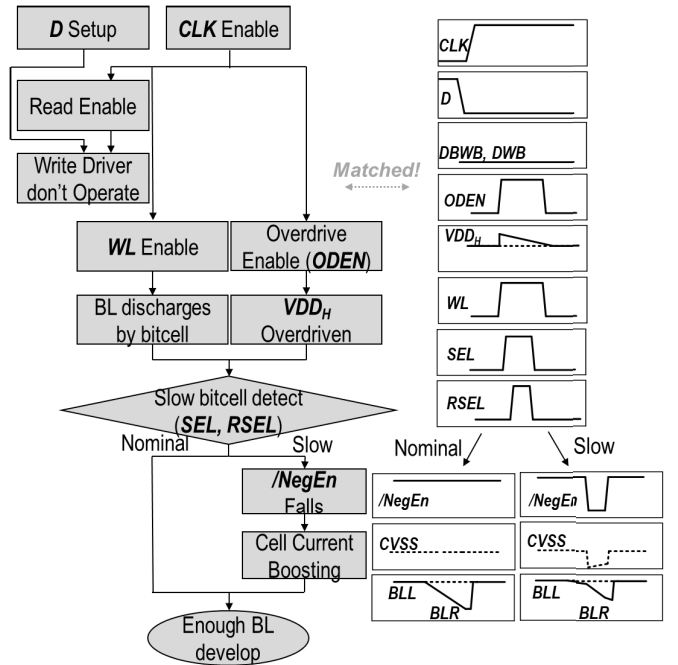


Fig. 11. Control signal flow chart of VBFD-SCCB and its matched waveforms.

with a standard deviation of $\sigma_{V_{th}}$, as indicated in the following equation (1) [26]:

$$\sigma_{V_{th}} = \frac{A_{\Delta V_t} / \sqrt{2}}{\sqrt{L_g W_g}} = \frac{A_{\Delta V_t} / \sqrt{2}}{\sqrt{L_g N_{fin} (2H_{fin} + T_{fin})}}, \quad (1)$$

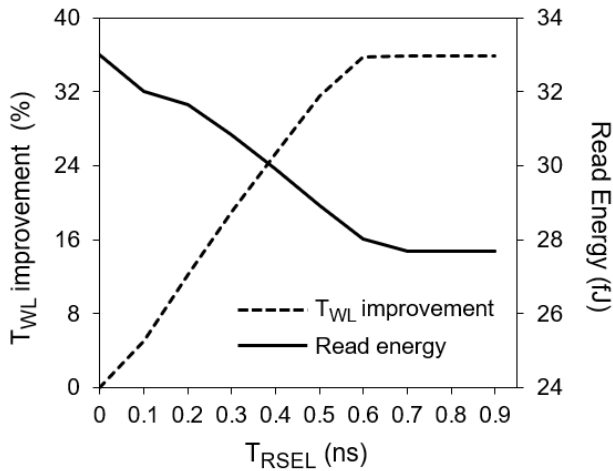


Fig. 12. T_{WL} improvement and read energy according to T_{RSEL} .

where $A_{\Delta V_t}$ is the Pelgrom coefficient, whose value is determined based on the silicon measurement results of 7nm FinFET in [27], and L_g , W_g , N_{fin} , H_{fin} , and T_{fin} are gate length, gate width, number of fins, fin height, and fin thickness in a FinFET, respectively.

Read stability yield and write ability yield are obtained based on the MPFP method [22]. That is because it is impossible to get a target read and write yield of 6σ with brute force MC simulation (~ 2000 years are needed). In addition, $T_{WL,6\sigma}$ is determined to meet the read sensing yield of 6σ , which is formulated by the following equation (2):

$$P[\Delta V_{BL}(T_{WL,6\sigma}) - V_{off} > 0] = CDF_{STD}(6), \quad (2)$$

where ΔV_{BL} is the voltage difference between the BL pairs, when at the time of $T_{WL,6\sigma}$, distribution of ΔV_{BL} is obtained by simulation and V_{off} is the sense amplifier offset voltage, it assumed that V_{off} follows the Gaussian distribution whose standard deviation is 30 mV [28], and $CDF_{STD}(Z)$ is the cumulative distribution function of the standard normal distribution. Thus, according to (2), to require target 6σ read sensing yield, it is said that $T_{WL,6\sigma}$ is quite related to the BL discharge speed. If one of BLs discharge slowly, $T_{WL,6\sigma}$ should be large. It should be noted that in the VBFD-SCCB circuit, $T_{WL,6\sigma}$ is got using simulation with importance sampling [24], [25], because BL distribution does not follow the gaussian distribution due to overdriving CVSS to a negative voltage.

Fig. 13 shows the Q-Q plot of T_{WL} distribution with conventional and VBFD-SCCB. In the low sigma region, which is near the nominal bitcell, BL discharging with VBFD-SCCB is slow compared to conventional circuits. This is because the effective resistance of CVSS is increased and capacitance is reduced owing to the use of the separated CVSS with the footer. Thus, the transient rise of CVSS during read operation is increased in VBFD-SCCB. However, as observed in the high sigma region which represents the slow bitcells that actually determine T_{WL} , the trigger of the proposed VBFD-SCCB effectively accelerates the BL discharging

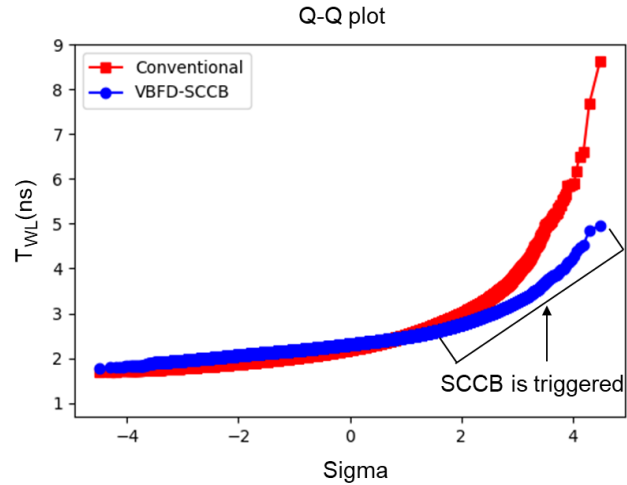


Fig. 13. Q-Q plot of T_{WL} distribution with conventional read and VBFD-SCCB.

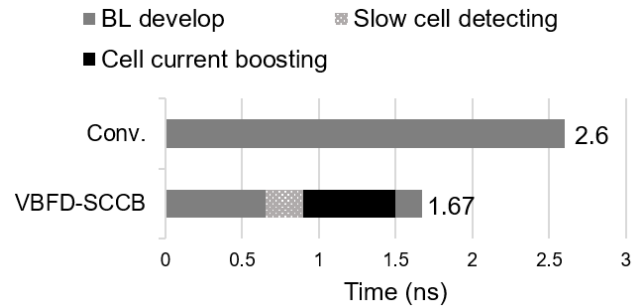


Fig. 14. The comparison of T_{WL} and its components with conventional and VBFD-SCCB read operation for the slow bitcell.

speed. By selectively boosting I_{CELL} , $T_{WL,6\sigma}$ can be improved by 36% compared with no assist circuit.

Fig. 14 shows the portion of T_{WL} for the conventional SRAM and the SRAM with the proposed VBFD-SCCB. In the conventional read operation, T_{WL} is determined by the BL development time (2.6 ns). In VBFD-SCCB, the BL development time, the slow bitcell detecting, and the I_{CELL} boosting are occupied by 39%, 15%, and 36% of whole T_{WL} (1.67 ns), respectively. Thus, T_{WL} of VBFD-SCCB is reduced due to I_{CELL} boosting even considering the additional circuit delay.

According to the simulation results, to the required target write yield of 6σ , the $C_{C1,6\sigma}$ value should be 12 fF for every four columns in the conventional structure. However, with the VBFD-SWA, the capacitance of BL is larger than the conventional structure because of added circuits like VBFD. Thus, the required $C_{C1,6\sigma}$ is 14 fF for four columns.

Table I summarizes the parameters and simulation results of comparison between conventional SRAM and proposed VBFD read and write assist SRAM. The capacitances of $C_{C1,6\sigma}$, C_{C0} , and C_S are implemented using the metal-oxide-metal (MOM) capacitor for high density and simplicity.

The area of one bitcell is 0.023 um^2 (width: 0.108 um, height: 0.216 um) in 7nm ASAP. The area of four columns bitcell array is 27.648 um^2 and the bitcell array with column

TABLE I
COMPARISON BETWEEN THE CONVENTIONAL AND
PROPOSED STRUCTURES

Method	Conventional	Proposed
V_{DD}	0.6 V	
$V_{WL,r6\sigma}$	0.52 V	
$T_{WL,r6\sigma}$	2.6 ns	1.67 ns
$C_{Cl,r6\sigma}$	12 fF	14 fF
Write-assist rate	100%	14%
Read energy for four columns	29.4 fJ	27.7 fJ 32.4 fJ (w/o RWL)
Write energy for four columns	39.5 fJ	31.8 fJ 34.5 fJ (w/o RWL)
Average energy	34.5 fJ	29.7 fJ
Area of bitcell (256×4)	27.648 μm^2	
Area of Column peri, I/O circuit	7.652 μm^2	11.85 μm^2
Total Area (4columns)	35.3 μm^2	39.5 μm^2

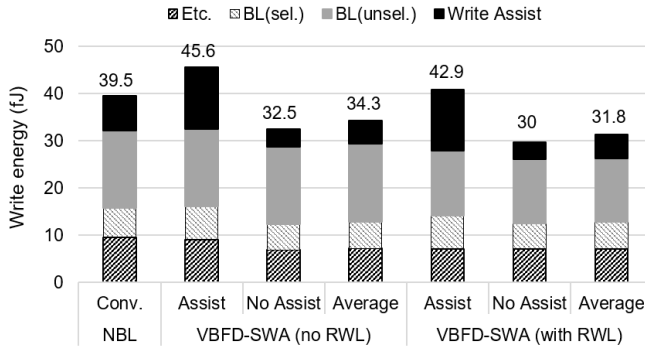


Fig. 15. Write energy consumption comparison when negative BL is used and when VBFD-SWA is applied without and with RWL.

peripheral circuit area is 39.5 μm^2 , where the peripheral circuit includes sense amplifier, column mux, write driver, I/O D-Latch, VBFD, and NVG with capacitors. Especially, capacitors occupy large portion of peripheral circuit area (C_{C1} : 7 μm^2 , C_{C0} : 0.75 μm^2 , C_S : 0.75 μm^2 , total: 8.5 μm^2). The total area overhead for a 256 × 4 SRAM array is 10% (35.3 μm^2 → 39.5 μm^2). In terms of PPA, by applying VBFD read and write assist circuits, the average power is improved by 14% (34.5 fJ → 29.7 fJ), and performance increased by 36% (2.6 ns → 1.67 ns), and the area overhead is 10%.

Fig. 15 shows the overall write energy comparison for four columns for the conventional NBL with a 12 fF coupling capacitor and the VBFD-SWA with a 14 fF coupling capacitor. Also, VBFD-SWA is categorized as with no RWL and with RWL. In VBFD-SWA, in the assist case, write energy is larger than conventional, whereas in the no assist case, the average energy saving of VBFD-SWA is about 13.1% (39.5 fJ → 34.3 fJ) and the selective write assist ratio is 14%. Applying the RWL in the VBFD-SWA, write energy is saved in every case. Thus, the energy saving is 19.4% (39.5 fJ → 31.8 fJ) with RWL.

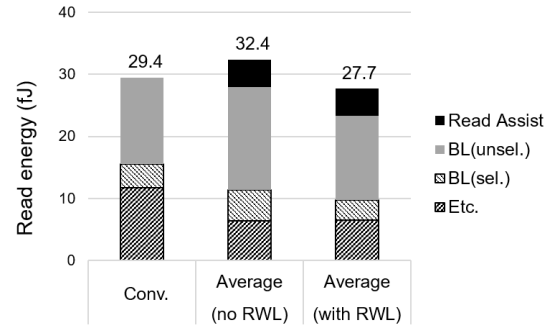


Fig. 16. Read energy consumption comparison when conventional read operation is used and when VBFD-SSCB is applied with and without RWL.

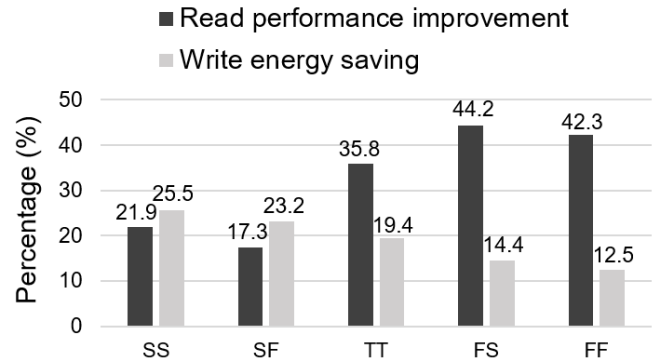


Fig. 17. Read performance improvement and write energy saving under the global corner variation.

Fig. 16 shows the average read energy comparison for four columns for the conventional SRAM read operation and the VBFD-SSCB. Because VBFD is added, the average energy of proposed circuits without reduced WL, increased compared with conventional 9.2% (29.4 fJ → 32.4 fJ), however applying RWL, the average read energy actually decreased by 5.8% (29.4 fJ → 27.7 fJ) owing to the elevated BL discharge level, even the circuit is more complicated.

If there is MOM capacitor size mismatch, the capacitor should be enlarged to satisfy the write yield. Assuming the worst capacitance variation of 5% [23], C_{C0} and C_S should be sized-up to 1.575 fF to have a 5% margin. In this condition, the area overhead is increased by 10.7% to 11.3%, and the average energy-saving effect is decreased by 13.9% to 13.1%.

Fig. 17 shows the read performance improvement rate and write energy saving rate when considering the global process corner. It shows that in fast nFET, the read performance improvement rate is high and the write energy saving rate is low. Conversely in slow nFET, the read performance rate is low and the write energy saving rate is high.

Due to the use of NBL, V_{MIN} can be improved by 190 mV, which is almost the same as the reported V_{MIN} results of 7nm FinFET SRAM having a similar configuration [29].

VI. CONCLUSION

VBFD-SWA and VBFD-SSCB are proposed for write assist and read assist, respectively. By detecting BL status, VBFD triggered the NVG for selective write assist and read assist, only when failure was detected. Selective write assist is

performed using VBFD-SWA to reduce write energy consumption. Also, by applying VBFD-SCCB, the read performance is significantly improved, and thanks to the reduced WL duration, the read energy is also decreased, whereas the circuits are complicated. The simulation results derived at the same V_{DD} condition indicated that the performance and energy consumption improved by 36% and 14%, respectively, by applying the proposed VBFD using circuits. However, the inevitable area overhead occurs at 10%.

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